# A DC to 40 GHz, High Linearity Monolithic GaAs Distributed Amplifier with Low DC Power Consumption as a High Bit-Rate Pre-Driver

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***Abstract* — This paper presents the design and the performance of a six stage GaAs MMIC distributed amplifier (DA) for optical driver applications. The DA is fabricated in a commercially available 0.15 µm GaAs p-HEMT technology. The amplifier exhibits 13 dB of small gain over 40 GHz of 3 dB bandwidth with a power consumption equal to 550 mW. Group delay time variation up to 30 GHz is only ±7 ps. The output power is higher than 16 dBm (4 $V_{pp}$), which makes the circuit suitable as a preamplifier for lithium-niobate ($LiNbO_3$) optical modulator driver. The DA is demonstrated as a part of the modulator driver in a 12.5 GBps PAM-4 (25Gbps) optical system by using the eye diagram as a figure of merit.**

***Keywords* — MMIC, Optical amplifier, Wideband amplifier, Distributed Amplifier, Traveling-wave amplifier, Optical Drives, Optical modulator, electro-optical modulation, $LiNbO_3$ modulator, pre-driver.**

## I. Introduction

Recently, the communication systems have undergone a major change in the bandwidth and in its transmission speed. In the case of optical communication systems speed per channel went up from 2.5 Gbps (OC-48) to 10 Gbps (OC-192) and even upper 40 Gbps (OC-768) [1]. That change has been a challenge not only for its optical part, but also for the analog circuits. In [2], it has been shown that a bandwidth of 0.5Rb to 0.7Rb, where Rb is bit rate, is the optimal solution for the bandwidth. Consequently, in the case of 40 Gbps optical systems the analog circuits require a flat response up to 28 GHz.

One of the most critical components in the analog part of the optical transmission system is the amplifier, which must rise the output signal from the multiplexer to an adequate value to drive the modulator of the system. This amplifier needs to have several decades of bandwidth and low group delay variation in order to limit the distortion of the waveform [3]. Monolithic distributed amplifier (DA) has been demonstrated as an optimum choice for such amplifier [4]. Despite the large size in comparison to other amplifier structures with the same gain, the DA is capable of providing a uniform gain in a huge bandwidth (more than one decade) as well as a good noise figure and a good input/output matching.

In the optical systems where the bit rate exceeded the 10 Gbps, the use of the external modulators becomes necessary to modulate the optical carrier. This kind of modulator is realized either as Electro Absorption Modulators (EAMs) or as Electro Optic Modulators (EOMs) for which the lithium-niobate is commonly used. Typically, the $LiNbO_3$ Mach-Zehnder Modulator (MZM) requires a drive level about 6Vpp.

In this paper, we describe the realization and the verification through experimental measurements of a six cells distributed amplifier based on a GaAs p-HEMT technology suitable as a preamplifier for 40 Gbps optical modulator driver. The design requirements include large bandwidth operating domain from DC to 40 GHz, small gain about 12 dB, low DC power consumption and a low group delay time variation in order to achieve low time jitter and a good eye-opening.

## II. DA Design

The distributed amplifier was fabricated using a low noise 0.15 µm pseudomorphic GaAs HEMT process with $f_t$ of 100 GHz, with -0.7 V of pinch-off voltage and 9 V of breakdown voltage. The optimum transconductance of the device is 580 mS/mm.

The simplified topology of the amplifier is shown in Fig. 1. The gain cell consists in two transistors with the same gate width of 30 µm and double gate fingers configuration, which are connected in cascode architecture.

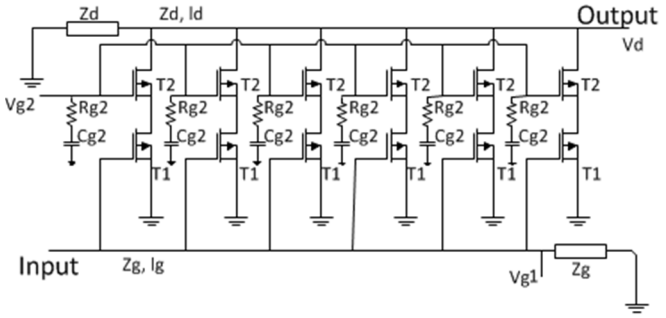


Fig. 1. Electrical schematic for the distributed amplifier.

The cascode gain cells of the distributed amplifier have significant advantages over the common source topology:

1) The output impedance of the cascode topology may be reduced at high frequency and, therefore, the drain losses can be compensated and thereby improving the gain.

2) The Miller effect may be reduced, which has the potential to increase the bandwidth, the isolation between the input and output transmission lines and also to improve the gain ripple.

However, it is necessary to pay special attention during the cascode distributed amplifier design process since the output resistance may become negative near the cutoff frequency which would cause the instability of the DA. Using the resistor $R_{g2}$ in serial with a small capacitor in the gate of the second transistor ($C_{g2}$) helps to decrease the maximum value of this impedance and also to increase the bandwidth of the DA [5].

In addition, during the design process it was possible to verify that the cascode topology of the gain cell allows to reduce the variation of the group delay time with respect to the common source transistor. This fact is represented in Fig. 2, where we can observe the group delay of a common source transistor (2x25 µm) and of two transistors of equal size and polarization point which are connected in cascode architecture. The common source transistor provides a variation of the group delay of 9 ps, while the cascode topology has a variation of 6.5 ps. Therefore, the variation of the group delay time is reduced by 2.5 ps.

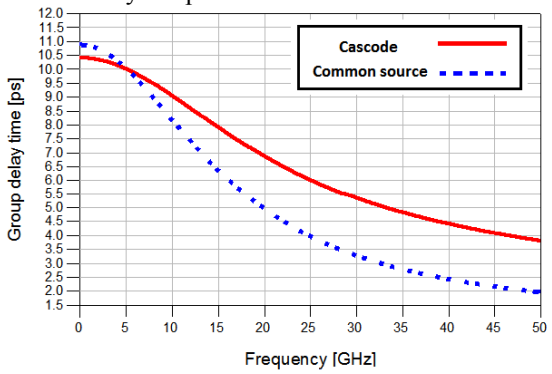


Fig. 2. Group delay versus frequency for the common source and cascode topology of the gain cell.

The effect of the transistor size of the cascode topology on the group delay time is shown in Fig. 3. By inspection of these figure, an increase in the gate size of the transistor implies the raise of the group delay time variation. It has also been proven that the components introduced in the gain cell to improve the stability of the amplifier ($R_{g2}$, $C_{g2}$), have no effect on the parameter under discussion.

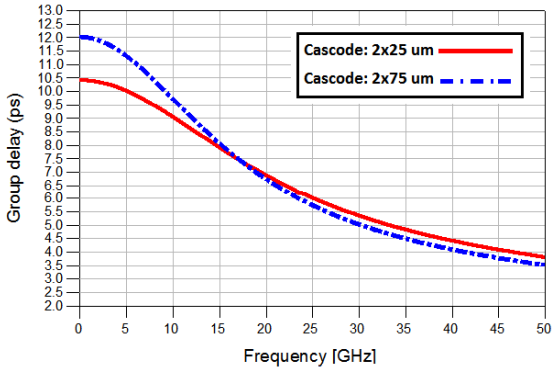


Fig. 3. Group delay versus frequency for the cascode topology with gate width of 25 µm and 75 µm.

The final proposed topology of the DA is shown in Fig. 4 where the six gain cells and also the drain and gate transmission lines as well as their load impedances can clearly be distinguished.

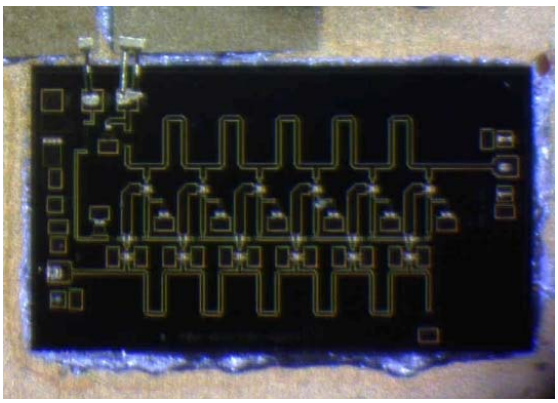

Fig. 4. Microphotograph of the fabricated distributed amplifier (2.3x1.3mm$^2$).

## III. Measurement Results

The microphotograph of the DA chip is shown in Fig. 4. The chip size is 2.3x1.3 mm$^2$. The amplifier was fed with a drain voltage of 3.3 V, the current consumption was 110 mA, which equals a power consumption of 0.36 W.

In order to control the low frequency response of the distributed amplifier, external bypass components are wire bonded to the drain and gate terminations in a similar manner to that described in [6]. For a better match between the simulations and the measurements, it is important to take into account a complex model of the external capacitors which are part of the bypass circuits. Indeed, this has been taken up in the parameters which are included in this paper.

The simulated and measured small gain of the amplifier is shown in Fig. 5.

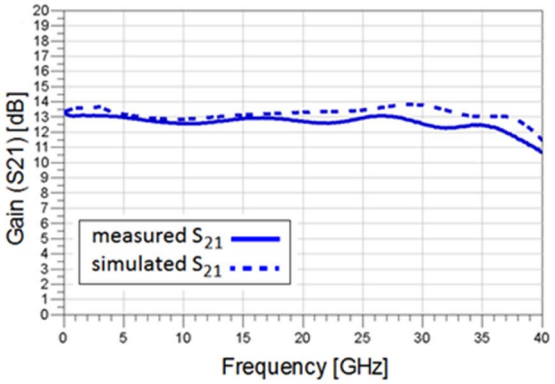


Fig. 5. Simulated and measured small gain of the distributed amplifier.

The measured small gain of the distributed amplifier is 13 dB with a corresponding -3 dB bandwidth of 40 GHz. The gain ripple is ± 1 dB up to 37 GHz. The gain and the bandwidth of the distributed amplifier allows to use it as a pre-driver for 40 Gbps $LiNbO_3$ modulator drivers, in the same form described previously in [7].

The input and output matching (Fig. 6) is better than -14 dB up to 40 GHz and -11 dB up to 40 GHz, respectively.

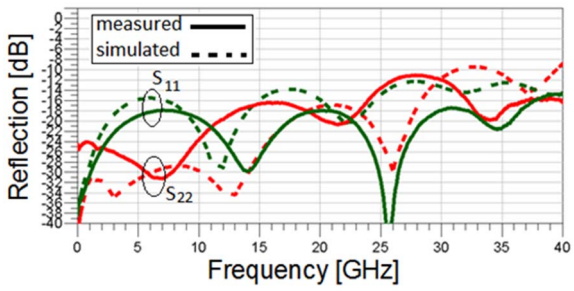


Fig. 6. Simulated and measured input and output matching for the DA.

In high speed optical systems, the variation of the group delay has an important impact in the jitter and in the good horizontal eye opening [8]. A comparison between the simulation and the measured group delay for the DA is shown in Fig. 7. Up to 30 GHz the measured group delay time variation (GDV) is very small and equals ±7 ps and the mean value is 50 ps. Along the whole measured bandwidth, the variation is ±18.5 ps.

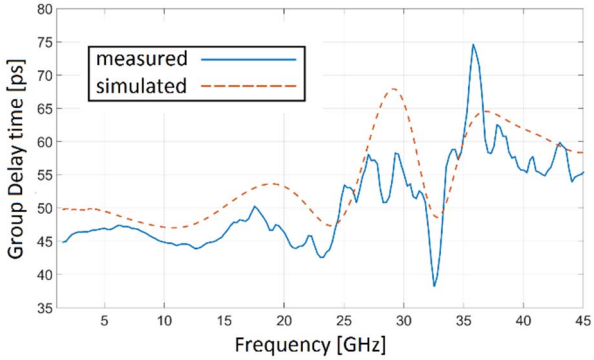


Fig. 7. Simulated and measured group delay versus frequency for the DA.

The saturated output power and the output power at 1dB gain compression point for the DA are shown in Fig. 8. Up to 30 GHz the measured saturated output power is 19 dBm ± 0.6 dBm. This is equivalent to 5.6 V peak to peak output voltage at a 50 Ω load. The DA shows a measured 1 dB gain compression point up to 30 GHz of 16 dBm ± 1 dBm, which is equivalent to 4 $V_{pp}$ at a 50 Ω load. Then, the amplifier can provide 2 $V_{pp}$, working in the linear regime, which is sufficient to drive the second stage of the optical driver.

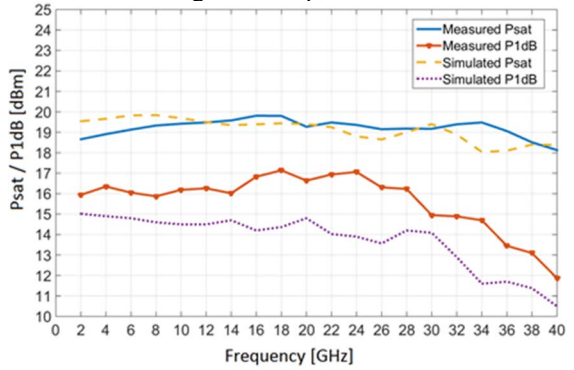


Fig. 8. Saturated Output Power (Psat) and Output Power at 1 dB gain compression point (P1dB) simulations and measurements for the driver.

Normally, the eye diagram is used as a figure of merit in the optical systems. For that reason, the distributed amplifier is used as a part of a modulator driver in a 12.5 GBps PAM-4 (25 Gbps) transmission experiment. Fig. 9 shows the electrical eye diagram at the output of the complete driver in linear operation. The amplitude of the waveform is about 2.3 $V_{pp}$ with a good eye-opening with low ripple inside the eye.

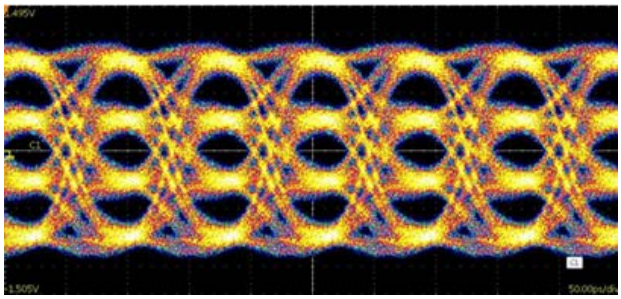

Fig. 9. Measured eye-diagram for PAM-4 at 12.5 GBps (25 Gbps).

## IV. Conclusion

In this paper we have presented the design and measurement results of a low DC power consumption six stages distributed amplifier using 0.15 µm GaAs technology.

During the design process we have verified that the topology of the DA gain cell has a great influence on the group delay time variation, checking that the cascode topology allows to reduce these variation. In addition, it has been proven that greater the size of the transistors, greater the variation of the group delay. Therefore, the best option to reduce the group delay time variation is to use a cascode topology with small gate transistors as a gain cell of the DA.

Table 1 summarizes the main performance parameters of previous GaAs distributed amplifier compared to the DA performance of this work. By inspection of the table, the amplifier of this work achieves comparable, even better, results than the prior distributed amplifier, especially when taken into account the low DC power consumption. Measured results demonstrate a mean value of gain of 13 dB over the bandwidth exceeding 40 GHz. The group delay time variation is only ±7 ps up to 30 GHz.

The performance of the device makes it suitable as a pre-driver for high bit-rate $LiNbO_3$ Mach-Zehnder Modulator, which was demonstrated in a PAM-4 transmission experiment.

## Acknowledgment

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Table 1. Performance comparison table of Distributed Amplifier for optical Drivers

| Ref. | Technology | 3dB Bandwidth (GHz) | Gain (dB) | Consumption (W) | Psat (dBm) | P1dB (dBm) | GDV (ps) |
|---|---|---|---|---|---|---|---|
| [1] | GaAs | 50 | 11.3 | 0.23 | - | 10.6 | ±7.5 |
| [3] | GaAs | 50 | 12.5 | 0.4 | - | - | ±7 |
| [7] | GaAs | 40 | 15.8 | 1.26 | 22.5 | - | - |
| [7] | GaAs | 43 | 10.7 | 0.47 | 19 | - | - |
| [8] | GaAs | 38 | 10.5 | 2.6 | - | 24 | ±15 |
| [9] | GaAs | 65 | 8 | 0.55 | - | - | ±3 |
| [9] | GaAs | 55 | 13 | 1.4 | - | - | ±8 |
| [10] | CMOS | 28.2 | 17 | 0.65 | - | - | - |
| [11] | SiGe BiCMOS | 90 | 12.5 | 0.55 | 14 | - | ±5 (up to 65 GHz) |
| [12] | SiGe BiCMOS | 70 | 14.5 | 1.1 | 12 | - | - |
| **This work** | **GaAs** | **40** | **13** | **0.36** | **19** | **16** | **±7** |

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